PROGRAM CONTROL

Introduction to the content

Instructions are always stored in successive memory locations.

Each time an instruction is fetched from memory, the program counter is incremented so that it contains the address of the next instruction in sequence.

Specifically, program control instruction when executed may change the address value in program counter and cause the flow of control to be altered.

Name	Mnemonic
BRANCH	BR
JUMP	JMP
SKIP	SKP
CALL	CALL
RETURN	RET
COMPARE	CMP
TEST	TST

1. BR/JMP-used interchangably to mean the same thing, but sometimes they are used to denote addressing mode. It may be conditional (branch if + or -)or unconditional (branch without any conditions)
2. Skip –does not need address field, it is a zero address instruction. Conditional skip instr. Will skip the next instr. In program counter.
3. Call and return are used in conjunction with subroutine.
4. The compare and test instr. Do not change the program sequence directly. The compare instr. Subtracts two operands, Certain status bits are set as a result. Test instr. Performs logical AND of two operands and updates certain status bits.

Topics in Program Control

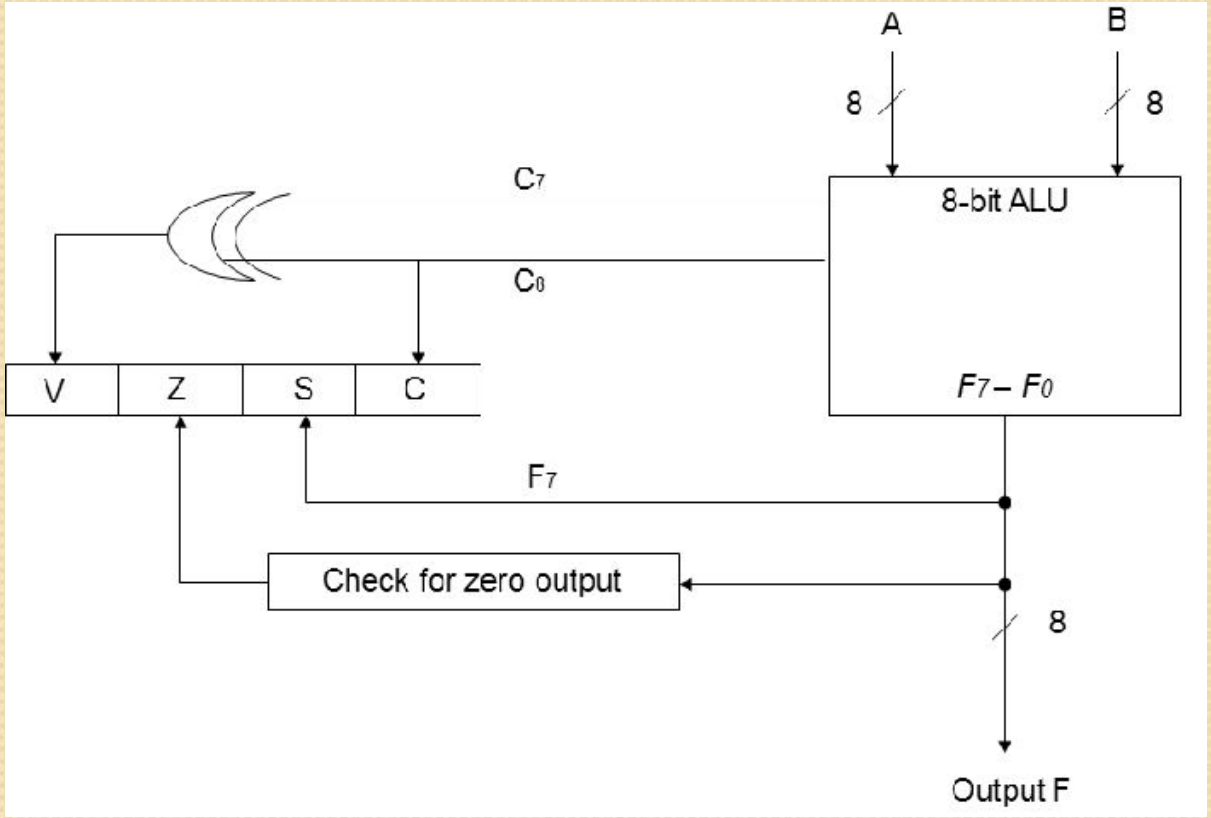
- Status bit conditions
- Conditional Branch Instructions
- Subroutine Call and Return
- Program interrupt & types

status bit conditions

The status register is a hardware register that contains information about the state of the processor..

The status register lets an instruction take action contingent on the outcome of a previous instruction.

The status register in a traditional processor design includes at least three central flags: Zero, Carry, and Overflow, which are set or cleared automatically as effects of arithmetic and bit manipulation operations.
Status bits are also called condition-code bits or flag bits.



1. Bit C (Carry): set to 1 if end carry c8 is 1, otherwise 0
2. Bit S (sign): Set to 1 ,if highest order bit F7 is 1, otherwise it is 0.
3. Bit Z (zero): Set to 1 if the output of ALU containts all o's, otherwise it is 0.
4. Bit V (overflow):, it is set to 1, if ex-or of last two carries is equal to 1,otherwise cleared to 0.

What are conditional branch instructions?

The term branching can be used when referring to programs in high level languages as well as program written in machine code or assembly language.

In high-level programming languages, branches usually take the form of conditional statements of various forms that encapsulate the instruction sequence that will be executed if the conditions are satisfied..

Machine level branch instructions are sometimes called jump instructions.

CONDITIONAL BRANCH INSTRUCTIONS

Mnemonic	Branch condition	Tested condition
BZ	Branch if zero	Z = 1
BNZ	Branch if not zero	Z = 0
BC	Branch if carry	C = 1
BNC	Branch if no carry	C = 0
BP	Branch if plus	S = 0
BM	Branch if minus	S = 1
BV	Branch if overflow	V = 1
BNV	Branch if no overflow	V = 0
	Unsigned **compare conditions (A - B)**	
BHI	Branch if higher	A > B
BHE	Branch if higher or equal	A ≥ B
BLO	Branch if lower	A < B
BLOE	Branch if lower or equal	A ≤ B
BE	Branch if equal	A = B
BNE	Branch if not equal	A ≠ B
	Signed **compare conditions (A - B)**	
BGT	Branch if greater than	A > B
BGE	Branch if greater or equal	A ≥ B
BLT	Branch if less than	A < B
BLE	Branch if less or equal	A ≤ B
BE	Branch if equal	A = B
BNE	Branch if not equal	A ≠ B

conditional branch instructions

- Each mnemonic is constructed with letter B (branch) and N(for no) inserted to define 0.
- The conditional instruction can be associated also with jump,skip,call or return type of program control instruction.
- The zero status bit is used for testing if the result of an ALU operation is equal to zero or not.

Subroutine Call

- A subroutine is a self-contained sequence of instructions that perform a given computational task.

During the execution of a program , a subroutine may be called to perform its function many times at various points.

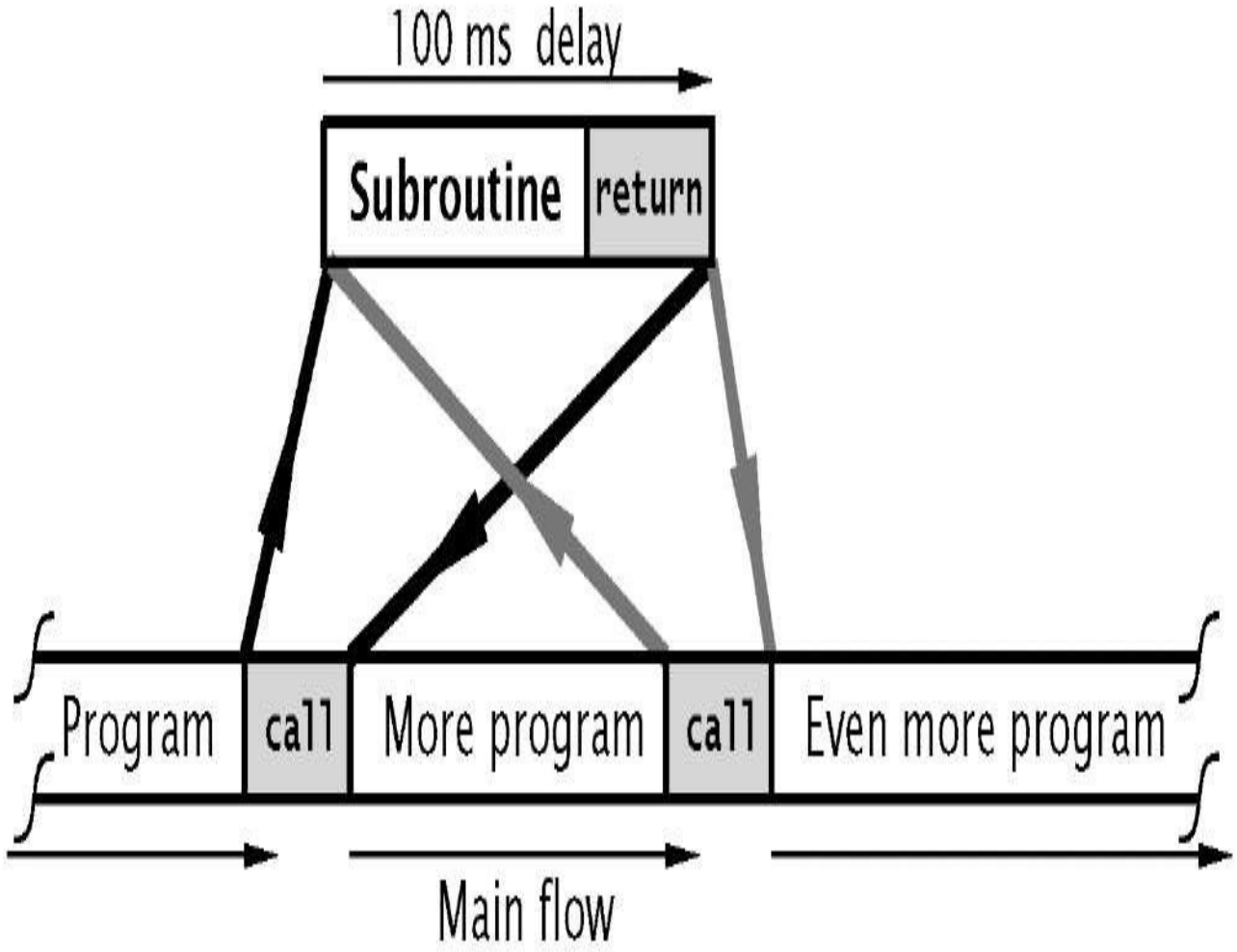
Subroutine Return

The subroutine may return a computed value to its caller (its return value), or provide various result values or output parameters.

A subroutine call may also have side effects such as modifying data structures in a computer memory, reading from or writing to a peripheral device, creating a file, halting the program or the machine,or even delaying the program's execution for a specified timeout

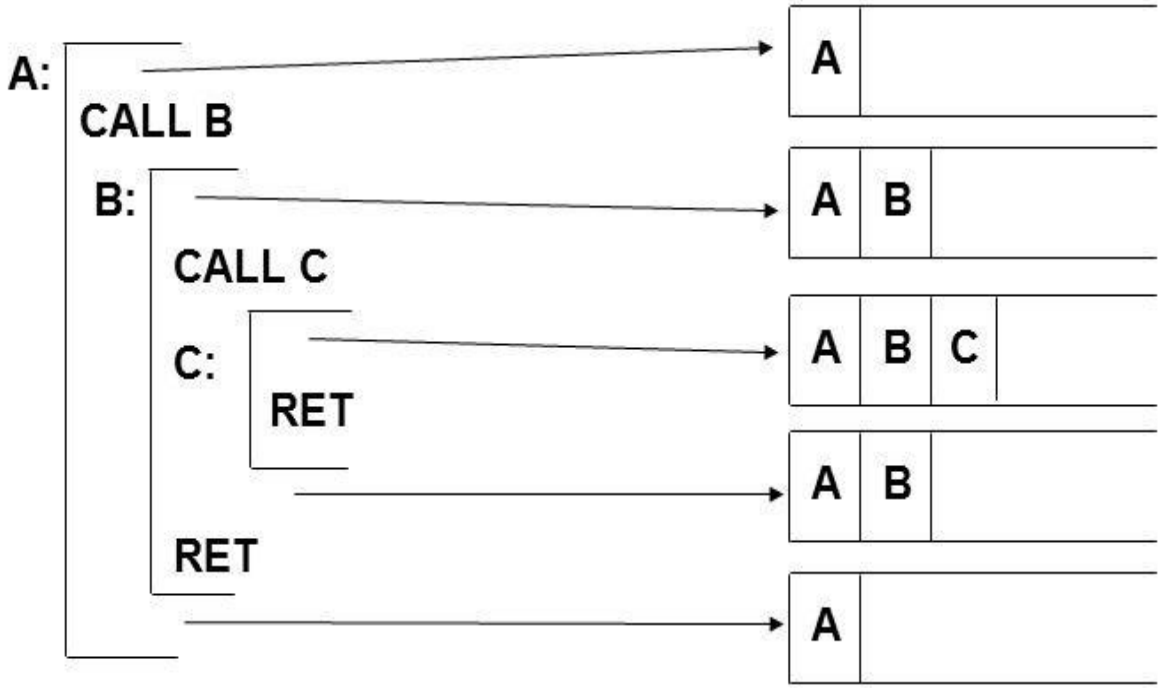
Subroutine Return

- The instr. From PC to a subroutine is known by different names.
- Call subroutine-consists of an operation code together with an address that specifies the beginning of the subroutine.
- Return from subroutine-it is the last instruction from subroutine, transfers the return address from temporary location into the PC.
- Branch to subroutine or recursive subroutine is a subroutine that calls itself. If only one register or memory location is used to store the return address, and the recursive subroutine calls itself, it destroys the previous return address


100 ms delay
Subroutine
return
Program
call
More program
call
Even more program
Main flow

Subroutine Calls

Stacking of Subroutine Calls & Returns and Environments:



Program Interrupt

- When a Process is executed by the CPU and when a user Request for another Process then this will create disturbance for the Running Process.This is also called as the **Interrupt**.
- Interrupts can be generated by User, Some Error Conditions and also by Software's and the hardware's. So that When an interrupt has Occurred then the CPU will handle by using the Fetch, decode and Execute Operations.
- Interrupts allow the operating system to take notice of an external event, such as a mouse click.
- The collection of all status bit conditions in the CPU is sometimes called a program status word or PSW.

Supervisor Mode

- When the CPU is executing a program that is part of OS, it is said to be in the supervisor mode or user mode.
- The execution mode on some processors which enables execution of all instructions, including privileged instructions.
- It may also give access to a different address space, to memory management hardware and to other peripherals.
- This is the mode in which the operating system usually runs.
- In computer terms, supervisor mode is a hardware-mediated flag which can be changed by code running in system-level software.

Types of program interrupt

- External
- Internal
- Software

External Interrupts

They come from I/O devices, from a timing device, from a circuit monitoring the power supply, or from any other external source.

Timeout interrupt may result from a program that is an endless loop and thus exceeded its time allocation.

It is asynchronous

Internal Interrupts

They arise from illegal use of an instruction or date.They are also calledTRAPS.

These erros occur due as a result of premature termination of the instruction execution.

The service program that processes the internal interrupt determines the corrective measure to be taken.

It is caused by the program itself, not by external event. It is synchronous

Software interrupts

It is a special instruction that behaves like an interrupt rather than a subroutine call.

It can be used by the programmer to initiate an interrupt procedure at any desired point in the program.

It is mainly used in supervisor mode.

THANKYOU