VLSI Design and Automation Lab

This lab helps to simulate and design any digital logic function in Verilog HDL. The various levels of abstraction level such as data flow, structural and behavioral can be modeled using existing facilities in the VLSI lab. It helps to realize combinational as well as sequential designs. The simulated code can be embedded on the Field Programmable Gate Array (FPGA) hardware boards for implementation. Dr.S.Vijaya Kumar had submitted a proposal for AICTE under the title “Analysis and Implementation of energy recycling model using HOMER (Hybrid Optimization model for Electric Renewable) and DC Alternators”.