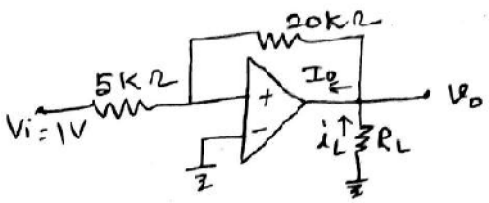
SREENIVASA INSTITUTE OF TECHNOLOGY AND MANAGEMENT STUDIES

(Autonomous)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

QUESTION BANK

20ECE243 – LINEAR AND DIGITAL IC APPLICATIONS

Question No.	Questions	PO Attainment
	UNIT – 1: BASICS OF OPERATIONAL AMPLIFIER	
	PART A (2 Marks)	
1	Define linear integrated circuits.	PO1
2	What are the ideal characteristics of op-amp?	PO1
3	Classify ICs on the basis of fabrication technology.	PO1
4	Mention different available IC package configurations	PO1
5	Classify ICs on the basis of chip size.	PO1
6	Define slew rate.	PO1
7	Define CMRR.	PO1
8	For the circuit shown below, calculate Vo, A_{CL} , load current i_L and output current i_0 	PO2
9	Identify some advantages of ICs over discrete circuits	PO1
10	Write some applications of ICs.	PO1
11	What is the gain of a non-inverting amplifier?	PO1
12	Draw the circuit diagram of an integrator and give its output equation.	PO1
13	Design an amplifier with a gain of –10 and input resistance of 10k ohm .	PO2
14	List the four non ideal dc characteristics of OP-Amp.	PO2
15	List the basic blocks of an operational amplifier.	PO1
	PART-B (10 Marks)	
1	Draw the circuits for inverting and non-inverting amplifier using op-amp. Also derive the expression for gain	PO2
2	Explain the circuits of differential amplifier using op-amp. Also derive the expression for gain, output voltage in terms of common mode and differential mode signals	PO2
3	Demonstrate the concepts of ideal and practical integrator circuit using op-amp.	PO2
4	Demonstrate the concepts of ideal and practical differentiator circuit using op-amp.	PO2
5	Sketch the implementation of instrumentation amplifiers using three op-amps. Also explain the principle of operation and its applications.	PO1
6	Explain the working principle of V/I and I/V convertor.	PO2
7	Write brief note on frequency compensation techniques applicable to operational amplifiers.	PO2
8	Discuss in detail about the DC characteristics of op-amp.	PO2
9	Describe the AC characteristics of operational amplifier.	PO2
10	For inverting amplifier with gain of -10, input resistance=10k ohm, Vi=1 V, R_L= 25 K ohm, calculate input current, output voltage, load current and total output current into the output pin.	PO2
11	Define input bias current and sate its effect on op-amp performance .explain how input bias current compensation is obtained.	PO2

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Question No.	Questions	PO Attainment
UNIT – 2: NON-LINEAR APPLICATIONS OF OP- AMPS		
PART A (2 Marks)		
1	What is a precision diode? Draw the circuit diagram of a half wave precision rectifier with waveform.	PO1
2	List any four important applications of a comparator.	PO1
3	Mention some advantages of active filters?	PO1
4	Define cutoff frequency?	PO1
5	What is a zero crossing detector?	PO1
6	Define precision diode.	PO1
7	What are the different types of filters?	PO1
8	Draw the circuit diagram of log amplifier.	PO1
9	Draw the circuit of log amplifier using two-amps.	PO1
10	What is a series voltage regulator?	PO1
11	What is meant by band reject filter and draw its frequency response.	PO1
12	Outline the comparator circuit and its waveform using inverting amplifier.	PO1
PART-B (10 Marks)		
1	Design a first order butterworth low pass filter having upper cut-off frequency of 1KHz. and pass band gain of 2.	PO3
2	Describe the first order high pass filter with neat circuit diagram. Derive its frequency response and plot the same.	PO2
3	Explain the operation of astable multivibrator using IC 741 and derive an expression for output frequency.	PO2
4	Summarize the operation of monostable multivibrator using IC 741 and derive an expression for time period.	PO2
5	Demonstrate the operation of triangular waveform generator using IC 741 and derive an expression for output frequency.	PO2
6	With neat circuits, explain band pass, band reject and all pass filters.	PO2
7	Illustrate log and antilog amplifier circuits with necessary circuits and waveforms	PO2
8	Explain the operation of comparator using inverting and non-inverting amplifier.	PO2
9	Explain half wave and full wave rectifier with necessary diagram.	PO2
10	With a neat diagram, explain the working principle of IC 723 voltage regulator.	PO2

Question No.	Questions	PO Attainment
UNIT – 3: SPECIAL ICs and DATA CONVERTERS		
PART A (2 Marks)		
1	How does Schmitt trigger acts as a regenerative comparator?	PO1
2	Mention the drawbacks of binary weighted resistor DAC.	PO1
3	List the applications of PLL.	PO1
4	Mention the features of VCO?	PO1
5	Which is the fastest ADC? State reason.	PO1
6	Outline the functional block of IC 555.	PO1
7	An 8 bit DAC has a resolution of 20mV/bit. what is the analog output voltage for the digital input code 00010110(the MSB is the left most bit)?	PO1
8	Define resolution and accuracy of a DAC.	PO4
9	What is monostable multivibrator?	PO1

10	What is astable multivibrator?	PO1
11	List the basic blocks of IC555 timer	PO1
PART-B (10 Marks)		
1	Explain the operation of Dual slope ADC with neat illustration.	PO2
2	Illustrate the operation of successive approximation type ADC with neat illustration..	PO2
3	Demonstrate the operation of astable multivibrator configured around IC 555 Timer and derive an expression for output frequency.	PO2
4	Describe the operation of monostable multivibrator configured around IC 555 Timer and derive an expression for output frequency.	PO2
5	With neat circuit diagram, discuss R-2R ladder type D/A Converter.	PO2
6	Discuss the operation of Voltage Controlled Oscillator (VCO).	PO2
7	Draw and explain the functional diagram of IC 555 Timer.	PO2
8	Draw the block diagram of PLL and explain its operations.	PO2
9	Discuss the operation of schmitt trigger with necessary sketch.	PO2
10	Explain the operation of Counter type ADC with neat illustration	PO2
11	Design a monostable multivibrator with trigger pulse shaping which will drive an LED ON for 0.5 second each time it is pulsed.	PO3
12	A schmitt trigger with the upper threshold level V_{UT}=0V and hysteresis width V_H=0.2V converts a 1KHz sine wave of amplitude 4 V_{pp} into a square wave. Calculate the time duration of negative and positive portion of the output waveform.	PO4
13	Describe in detail about Analog multiplier with neat sketch	PO2

Question No.	Questions	PO Attainment
UNIT – 4: CMOS LOGIC & BIPOLAR LOGIC AND INTERFACING		
PART A (2 Marks)		
1	Classify the logic family by operation	PO1
2	Which is the fastest logic gate? And why?	PO1
3	Mention the DC noise margin levels of ECL 10K family	PO1
4	Give the logic levels and noise margins of CMOS and TTL families.	PO1
5	Define transition time with respect to CMOS logic.	PO1
6	What is the necessity of separate interfacing circuit to connect CMOS gate to TTL gate?	PO1
7	How the CMOS family is advantage over TTL family.	PO1
8	Sketch NAND gate circuit using CMOS transistor.	PO1
9	Draw NOR gate circuit using CMOS transistor.	PO1
10	Write the characteristics of logic family.	PO1
11	How TTL is classified based on output configuration?	PO1
12	Mention the advantages and disadvantages of CMOS technology.	PO1
PART-B (10 Marks)		
1	Explain the operation of ECL with neat circuits.	PO2
2	With neat diagram explain Bipolar logic with TTL	PO2
3	Explain the steady state electric behaviour of CMOS logic	PO2
4	Discuss about CMOS dynamic electrical behavior with characteristics.	PO2
5	Sketch the circuit diagram of two input 10K ECL OR/NOR gate and explain its function with the help of truth table.	PO2
6	Draw and explain the operation of a TTL NAND gate along with it truth table.	PO2
7	a) Implement the functions Y=(AB+CD)' using CMOS. b) Implement the functions Y=((A+B)(C+D))' using CMOS.	PO2

		PO2
8	a) Implement two input EX-OR gate using CMOS logic along with it truth table. b) Implement two input EX-NOR gate using CMOS logic along with it truth table.	PO2 PO2
9	Illustrate in detail about the power dissipation in CMOS inverter.	PO2
10	Implement two input NAND gate using TTL logic	PO2
11	a) Compare CMOS, TTL and ECL Families b) Implement two input OR gate using CMOS logic.	PO2 PO2

Question No.	Questions	PO Attainment
UNIT – 5: CPLDs and FPGAs		
PART A (2 Marks)		
1	Define CPLD	PO1
2	Draw the general architecture of CPLD	PO1
3	What is PLD?	PO1
4	List out the advantages of CPLD.	PO1
5	Define I/O block.	PO2
6	Draw the architecture of Xilinx 9500 CPLD	PO2
7	What is product term allocator?	PO2
8	Define Macrocell	PO2
9	Draw XC4000 general interconnect structure.	PO1
PART-B (10 Marks)		
1	Explain in detail about CPLD and draw necessary diagram.	PO2
2	Discuss in brief about interconnect matrix.	PO2
3	With a neat sketch, explain the architecture of Xilinx XC9500 CPLD	PO1
4	Describe the operation of Xilinx XC 4000 FPGA and draw the diagram wherever necessary.	PO1
5	Illustrate the functions of I/O block and CLB of XC9500 series	PO1
6	Explain in detail about I/O block and CLB in Xilinx XC4000 series	PO1
7	Explain function block architecture of XC 9500.	PO1