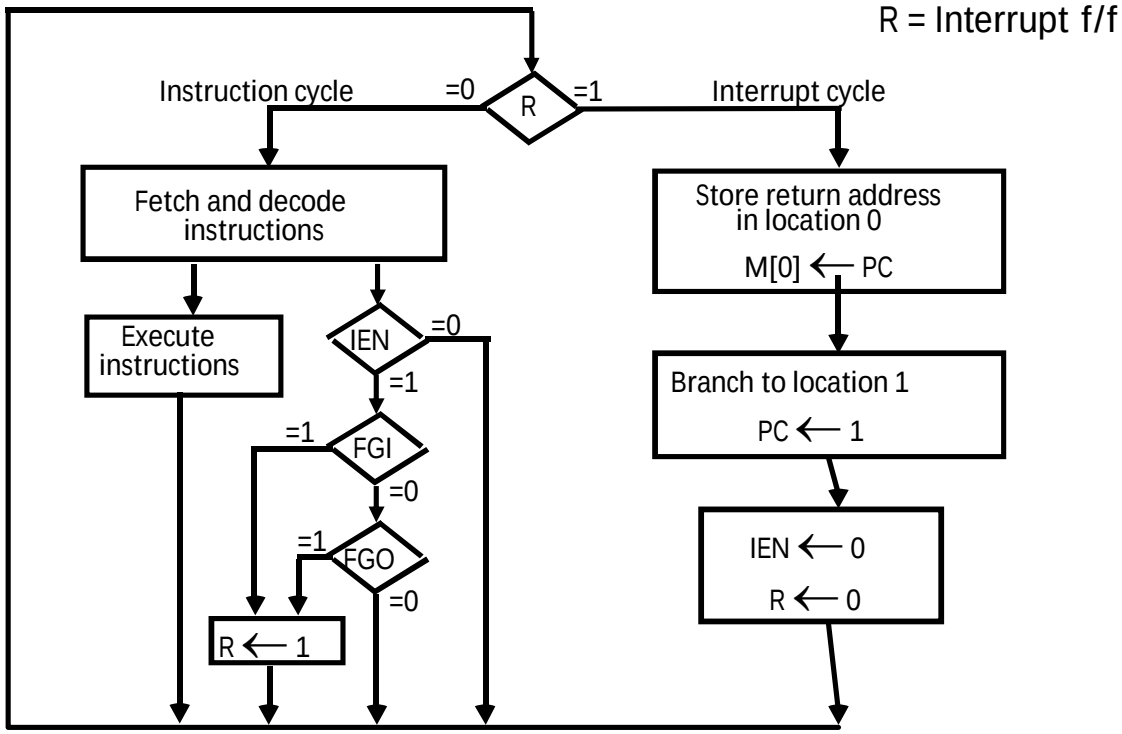
INTERRUPT

Interrupt

- **Interrupt** is a signal to the processor emitted by hardware or software indicating an event that needs immediate attention.
- The way the interrupt is handled by the computer can be given by the following flowchart:

FLOWCHART FOR INTERRUPT CYCLE



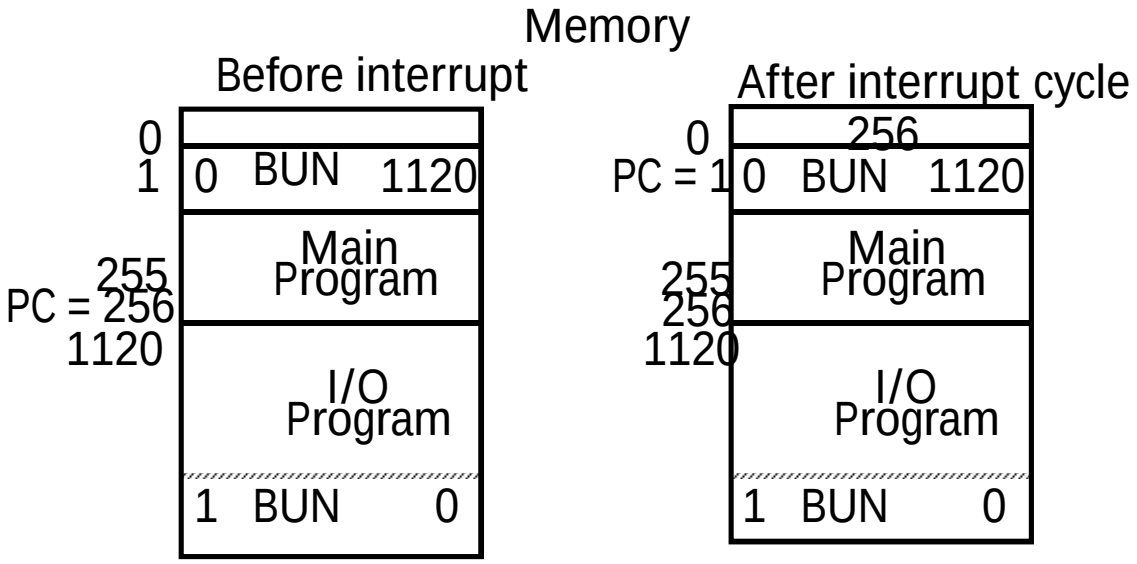
Interrupt cycle

- An interrupt flip flop R is included in the computer. When R=0 the computer goes to the instruction cycle.
- During the execution of instruction cycle, IEN is checked by control.
- If IEN is 0 it indicates that control continues with next cycle.
- If IEN is 1 the control checks flag bits, if both flags are 0, it indicates that neither i/p nor the o/p register are ready for transfer of information.
- If the either of flag is set to 1, when IEN=1, the flip flop R is set to 1 and it goes to interrupt cycle instead of instruction cycle in the next cycle.

Interrupt cycle

- The interrupt cycle is a HW implementation of a branch and save return address operation.
- The return address is available in PC and the same is stored at the address 0.
- Control then inserts address 1 into PC and clear IEN and R, So that no more interrupt can occur until interrupt request has been serviced.

INTERRUPT CYCLE WITH EXAMPLE



Interrupt cycle

- Suppose that interrupt occurs and R is set to 1 while the control is executing the instruction at address 255. At this time the return address 256 is in PC.
- The content of PC is stored in memory location 0, PC is set to 1.
- The branch instruction at address 1 causes the program to transfer to I/O service program at address 1120.
- After the execution of I/O service program, the control returns to the location where it was interrupted that is to address 256 in the main program.