## BCD M ultiplication and Division

## BCD Multiplication

- The register configuration for decimal multiplication is shown below



## BCD Multiplication

- Assuming here the 4 digit number with each digit occupying 4 bits for a total of 16 bits of each number.
- There are 3 registers $A, B$, and $Q$ each having corresponding flip-flops As, Bs and Qs.
- Registers $A$ and $B$ have four more bits designated by Ae and Be that provides an extension of one more digit to the registers.
- The BCD arithmetic unit adds five digit in parallel and places the sum in five digit A register and the end carry goes to E flip-flops.


## BCD Multiplication

- The least significant digit in register Q is designated by QL which is incremented or decremented.
- The decimal multiplication algorithm is shown below


## BCD Multiplication



Figure 10-22 Flowchare for decimal multiplication.

## BCD Multiplication

- Initially A register and Be are cleared and SC is set to a number $K$ equal to number of digits in multiplier.
- Least Significant digit of multiplier in QL is checked, if it is not equal to 0 , multiplicand in $B$ is added to partial product in A and QL is decremented.
- QL is checked again and process is repeated until it is equal to 0 .
- The partial product and multiplier are shifted once to the right and SC is decremented.
- The process is repeated K times to form double length product in AQ.


## BCD Division



Figure 10-23 Flowchart for decimal division.

## BCD Division

- The algorithm can be summarized as follows:

1. Load the divisor into $B$ register, dividend into $A Q$ register, $S C$ with $K$ number of digits in divisor and register Be cleared to zero.
2. Perform dshl AQ one time.
3. Perform the subtract operation

$$
\mathrm{EA} \leftarrow \mathrm{~A}+\mathrm{B}^{\prime}+1
$$

4. $E$ value is checked whether it is equal to 0 .
5. if it does $B$ is added back to $A, S C$ is decremented by one and control goes to step 8.

$$
A \leftarrow A+B
$$

6. Otherwise QL is incremented by 1 and perform the subtract operation

$$
\begin{aligned}
& \mathrm{QL}<\mathrm{QL}+1 \\
& \mathrm{EA} \leftarrow \mathrm{~A}+\mathrm{B}^{\prime}+1
\end{aligned}
$$

7. $E$ value is checked whether it is equal to 0 , if it does the control goes to step 5 otherwise the process in step 6 continues.
8. SC is checked, if it is not equal to 0 the control goes to step 3 otherwise process stops and quotient will be in Q and Remainder will be in A .
