Addition and Subtraction with Signed 2’s Complement Data

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- When two numbers of n digits are added, the sum occupies n+1 digits, then the overflow is occurred.
- The overflow can be detected by inspecting the last two carries out of addition.
- When two carries are applied to an XOR gate the overflow is detected when the o/p of the gate is equal to 1.

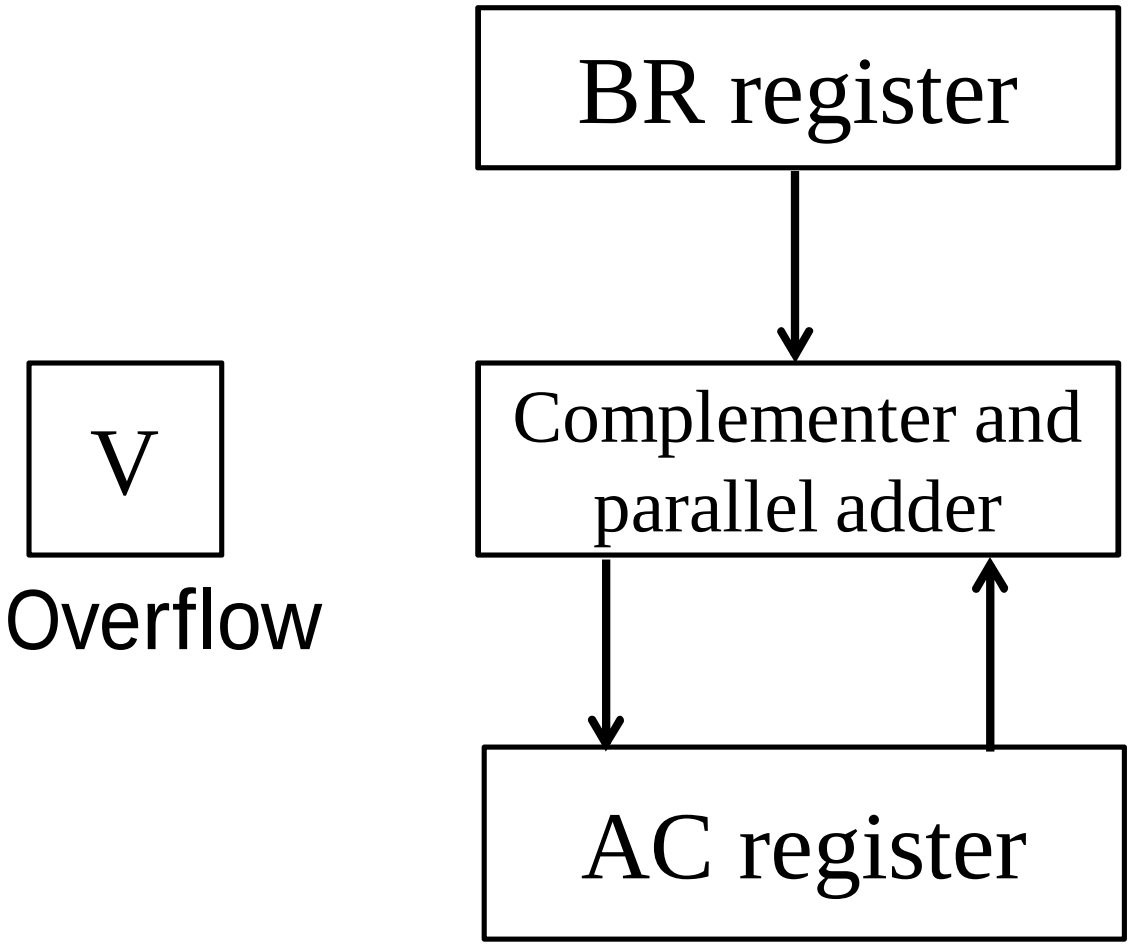

Figure: Hardware for signed-2's complement addition and subtraction.

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- The leftmost bit in AC and BR represents the sign bits of the number.
- The two sign bits are added or subtracted together with the other bits in the complementer and parallel adder.
- The overflow flipflop V is set to 1 if there is an overflow.
- The algorithm for adding and subtracting numbers using signed 2's complement representation is shown in the below flowchart.

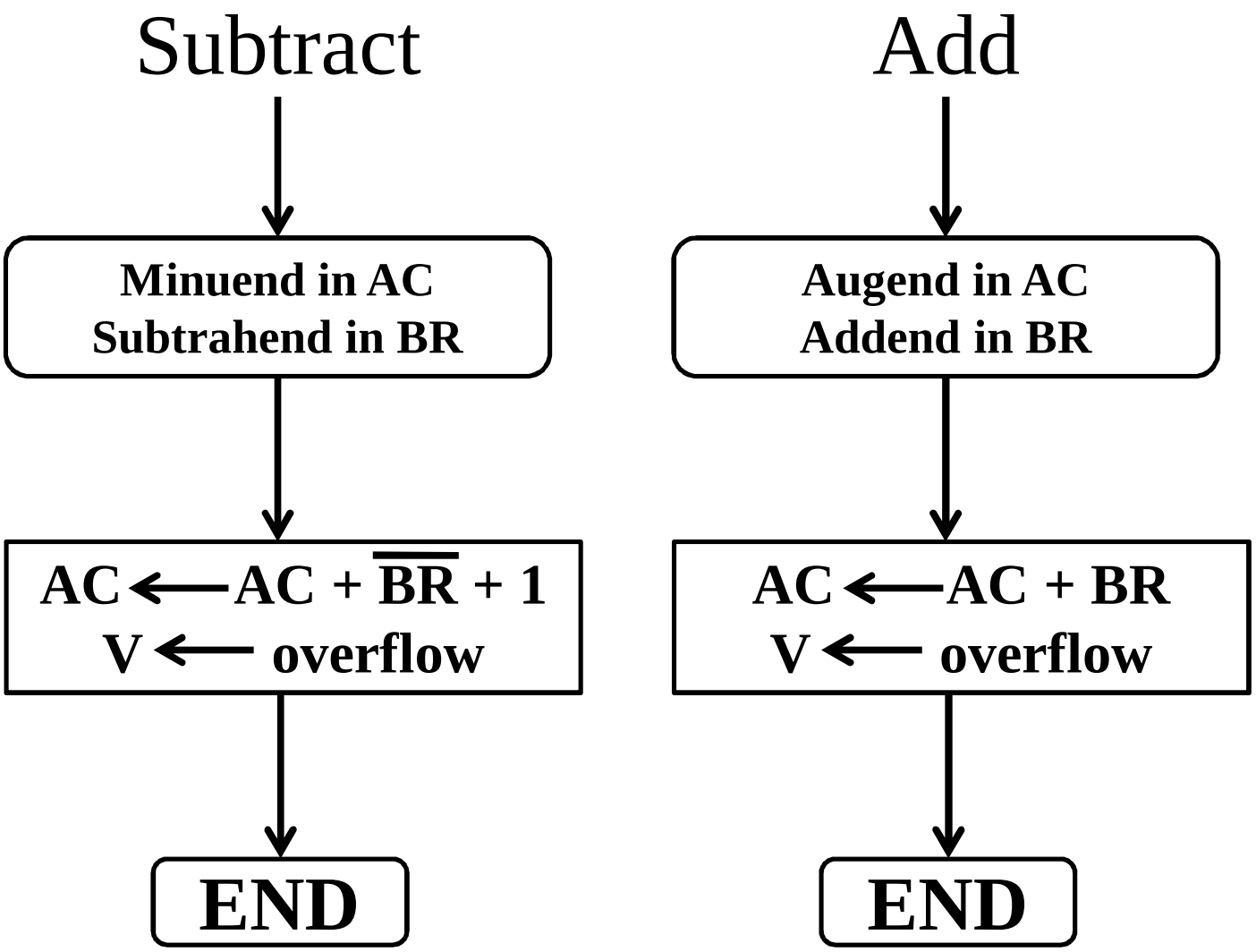

Figure: Algorithm for adding and subtracting numbers in signed-2's complement representation.

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- The sum is obtained by adding the content of AC and BR.
- The overflow bit is set to 1 if the XOR of last two carries is set to 1 otherwise to 0.
- The subtraction operation is obtained by adding the content of AC to the 2's complement of BR.
- Comparing this algorithm with signed magnitude, it is simpler to add and subtract numbers if negative numbers are in signed 2's complement form.
- So the most of the computers adopt this representation over signed magnitude form.