SREENIVASA INSTITUTE of TECHNOLOGY and MANAGEMENT STUDIES (AUTONOMOUS): CHITTOOR
DEPARTMENT 0f ELECTRONICS and COMMUNICATION ENGINEERING

II Year B.Tech. I semester

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16ECE 213 SWITCHING THEORY AND LOGIC DESIGN (Common to ECE & EEE)

Course Educational Objectives:

- To familiarize the students with different number systems, conversions, digital logic, simplification and minimization of Boolean functions.
- To design combinational & sequential digital circuits and state machines.
- To introduce programmable logic devices.

UNIT - 1: Number Systems& Codes

Review of Number Systems- Binary Arithmetic-subtraction with r and (r-1)'s Complements- Weighted & Non Weighted Codes- Error Detection and Error Correction Codes- Hamming Code.
Boolean Algebra : Boolean Theorems-Basic Logic Operations (NOT,OR,AND)-Complement and Dual of Logical Expressions- Universal Gates- EX-OR&EX-NOR Gates- Standard SOP and POS-Minimization of Logic Functions Using Theorems.

UNIT - 2: Minimization of Switching Functions

Minimization of Switching Functions Using K-Map Up to 5 variables-Tabular Minimization (Quine-Mcluskey)- Minimal SOP And POS Realization-Problem Solving Using K-Map for Boolean Functions in SOP and POS Forms.

UNIT - 3: Combinational Logic Circuits & PLD's

Combinational Logic Circuits:

Design of Half Adder - Full Adder - Half Subtractor- Full Subtractor- 4-bit binary adder-4-bit adder subtractor- BCD adder-carry look ahead adder -Magnitude Comparator – Decoder- Encoder- Priority Encoder – Multiplexer – De multiplexer – Code converters .

PLD's:

PROM – PLA – PAL ,Realization of Switching Functions Using PROM - PLA and PAL - Comparison of PROM, PLA, and PAL.

UNIT - 4: Sequential Circuits I

Classification of Sequential Circuits (Synchronous And Asynchronous)-Basic Latches & Flip Flops-SR, D, JK,T –Conversion between Flip Flops- Design of Shift Registers-Universal Shift Register.
Design of Synchronous and Asynchronous Counters.

UNIT - 5: Sequential Circuits II

Finite State Machine - Capabilities and Limitations- Analysis of Clocked Sequential Circuits-Design Procedures- Reduction of State Tables and State Assignment-Realization of Circuits Using Various Flip flops-Mealy and Moore State Machines- Introduction to ASM Charts with Examples

Course Outcomes:

- ✓ Simplify the logic expressions using Boolean laws and postulates and design them by using logic gates.
- ✓ Minimize the logic expressions using map method and tabular method. Design of combinational logic circuits using conventional gates.
- ✓ Become familiarize with FSM & ASM.

Text books:

1. Digital Design, 3/e,2006,Morris Mano,Prentice Hall of India, New Delhi.
2. Digital Fundamentals, 10/e,2008,ThomasL.Floyd,Pearson/Prentice Hall, New Delhi.

Reference books:

1. Fundamentals of Logic Design, 5/e, 2004,Charles H.Roth ,Thomas Publications, New Delhi.
2. Switching & Finite Automata Theory, 2/e, ,ZviKohavi,Tata McGraw Hill, NewDelhi.
3. Digital systems Principles And Applications, -8/e, 2002, Ronald J.Tocci Neal S.widmer, Pearson Education, New Delhi.